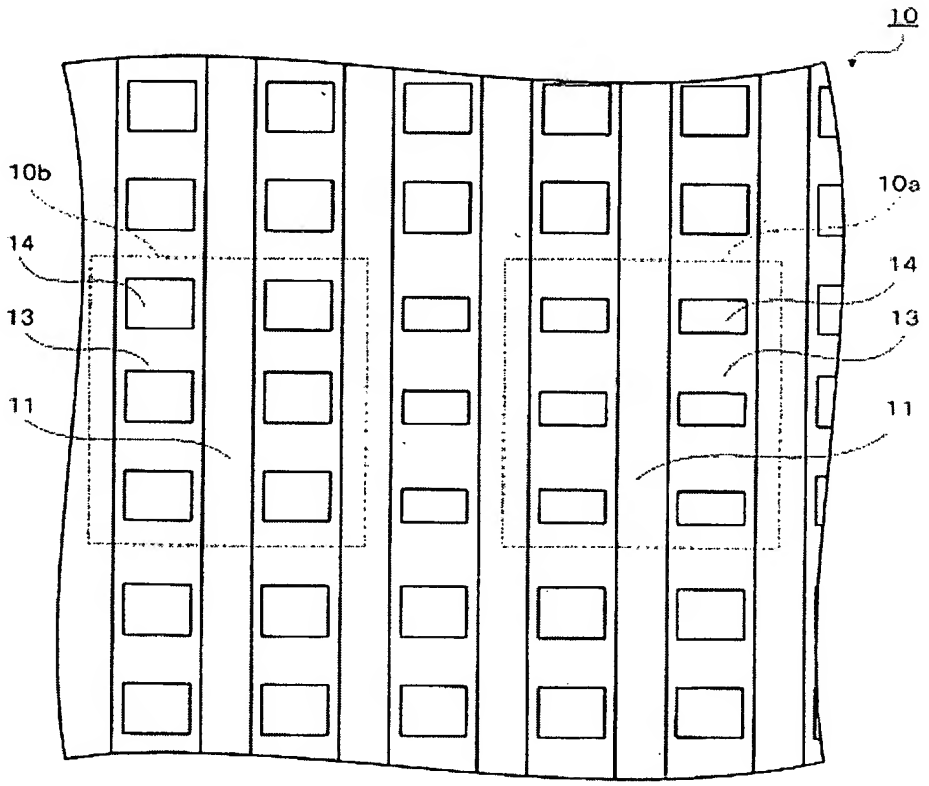
REMARKS/ARGUMENTS

Claim 1 is amended by this response. Claims 5-6 are canceled, and no claims are added. Following entry of these amendments and remarks, claims 1-4 will remain pending.

Claims 5-6 have been canceled as agreed upon in the interview on April 9, 2008 without prejudice to filling of continuation applications drawn thereto.

In the latest office action, the Examiner objected to FIG. 4. FIG. 4 is a cross-sectional view along line X-X of FIG. 2. This X-X line is not straight (level differences exist, as shown in the figure). Thus, only one side of an N+-type emitter region in Fig. 4 contacts a gate insulation film 34 and the like. Accordingly, Applicants respectfully maintain that FIG. 4 is in fact a correct depiction, and decline at this time to amend the drawings.

Turning now to address the claim rejections, embodiments of the invention relate to an insulated gate semiconductor device. The plan view of FIG. 1 (reproduced below) shows an embodiment where emitter regions 14 and base regions 13 formed on a semiconductor base 10.



In particular, a first region (10a) is formed at a center and on a surface of the semiconductor base 10, wherein the size of the emitter regions 14 is smaller. A second region

(10b) is formed at a circumference (peripheral part) and on a surface of the semiconductor base 10, such that it encloses the first region. Consistent with this description, FIG. 1 shows the size of the emitter regions 14 in center region (10a) as smaller than the size of the emitter 14 in the surrounding regions (region 10b, and other regions above, below, and to the right of region 10a.)

According to this configuration, the ratio of area of the N^+ type emitter region to the P^- type base region is small at the center part, where heat is likely to converge. Thus, a sufficient amount of current is supplied to the peripheral part, where heat does not converge, and a loss of current capacity can be minimized for the semiconductor device as a whole. As the amount of current flowing through the center part is smaller than that through the peripheral part, the heat occurring at the center part is smaller than that occurring at the peripheral part.

In this manner, a thermal runaway effect is not likely to occur at the center part of the semiconductor device, even when the heat generated at the peripheral part is transmitted and added to the heat generated at the center part.

Accordingly, claim 1 has now been amended to recite as follows:

> 1. A semiconductor device, comprising:
> a semiconductor base comprising a first semiconductor region having a first conductivity type, a second semiconductor region having a second conductivity type formed in a specific surface region of said first semiconductor region, and a third semiconductor region having the first conductivity type formed in a specific surface region of said second semiconductor region; and
> a first electrode formed on in a surface region of said second semiconductor region sandwiched between said first semiconductor region and said third semiconductor region,
> wherein: a first region, in which said third semiconductor region occupies said second semiconductor region at a first rate, is formed at a center of said semiconductor base, and
> a second region, in which said third semiconductor region occupies said second semiconductor region at a second rate larger than said first rate, is formed at a circumference of said semiconductor base so as to enclose said first region.
> (Emphasis added)

In the latest office action, the Examiner rejected claims 1-6 as indefinite under 35 U.S.C. §112 ¶2. As a threshold matter, Applicants note that the Examiner appears to be placing undue emphasis on technical, non-prior art rejections:

706.03 Rejections Not Based on Prior Art

> The primary object of the examination of an application is to determine whether or not the claims are patentable over the prior art. This consideration should not be relegated to a secondary position while undue emphasis is given to nonprior art or "technical" rejections. Effort in examining should be concentrated on truly essential matters, minimizing or eliminating effort on technical rejections which are not really critical. (Emphasis added)

The Examiner is respectfully reminded of the wide latitude afforded Applicants in their choice of claim terminology:

> A fundamental principle contained in 35 U.S.C. §112, ¶2 is that applicants are their own lexicographers. . . . Applicant may use functional language, alternative expressions, negative limitations, or any style of expression or format of claim . . . (Emphasis added; MPEP §2173.01)

Moreover, the MPEP directs the Examiner to:

> allow claims which define the patentable subject matter with a reasonable degree of particularity and distinctness. Some latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the examiner might desire. (Emphasis original; MPEP §2173.02)

Here, it is emphasized that the first region (at the center of a semiconductor base) and the second region (at the circumference of the semiconductor base) are not semiconductor regions (second and third semiconductor regions), but rather are specific regions on the semiconductor base. In particular, Applicants have provided more than enough description in the specification regarding the distinctions of different "regions", to satisfy the degree of reasonableness required by the MPEP.

For example, at least **¶[0008]** and **¶[0025]-¶[0026]** of the instant application discuss this aspect of the claim elements:

> ....a first semiconductor region having a first conductivity type, a second semiconductor region having a second conductivity type formed in a surface region of the first semiconductor region, and a third semiconductor region having the first conductivity type formed in a surface region of the second semiconductor region; and
>
> ***
>
> ....a first region, in which the third semiconductor region occupies the second semiconductor region at a first rate, is formed at a center of the semiconductor base, and a second region, in which the third semiconductor region occupies the second semiconductor region at a second rate larger than the first rate, is formed

> at a circumference of the semiconductor base so as to enclose the first region. **(¶[0008])**
>
> ***
>
> The N^- type base region 11 is formed of an N type semiconductor region in which an impurity of N type (first conductivity type) such as, for example, phosphorus, etc. is diffused. The N^- type base region 11 is formed so as to have, for example, a thickness of about 45 um, and an impurity concentration of about $2x10^{14}cm^{-3}$. The P^+ type collector region 12 is formed of a P type semiconductor region in which an impurity of P type (second conductivity type) such as, for example, boron, etc. is diffused, and is formed on the lower surface of the N type buffer region 15 as shown in FIG. 4. **(¶[0025]-¶[0026])**

The description of the above claim terms may not be as precise as the Examiner might desire. However, these claim terms are illustrated at FIG. 1 (reproduced above) and discussed at length in the accompanying text of the specification. Such disclosure certainly provides the reasonable degree of particularity and distinctness called for by the MPEP.

Regarding purported indefiniteness of the term "first electrode", claim 1 has been amended to clarify that a first electrode is formed in a surface region of the second semiconductor region which is sandwiched, on the surface region thereof (not in the vertical direction, but in the horizontal direction), between the first semiconductor region and the third semiconductor region. Also, the term "specific" is added to claim 1 to clarify that the second semiconductor region is not formed in the entire surface of the first semiconductor region. In view of these amendments and remarks, it is respectfully asserted that continued maintenance of the indefiniteness claim rejections is improper, and the claim rejections should be withdrawn.

Regarding claim rejections based on alleged prior art, claims 1-4 stand rejected as anticipated by JP Patent Application Publication No. 2004-228553 to Torii et al. ("the Torii Publication"). These claim rejections are overcome as follows.

As a threshold matter, the Examiner is respectfully reminded that all claims stand rejected as anticipated, and not merely obvious, in view of the Torii Publication:

> [t]he distinction between rejections based on 35 U.S.C. 102 and those based on 35 U.S.C. 103 should be kept in mind. Under the former, the claim is anticipated by the reference. No question of obviousness is present. In other words, for anticipation under 35 U.S.C. 102, the reference must teach <u>every aspect of the claimed invention either explicitly or impliedly</u>. Any feature not directly taught must be inherently present. (Emphasis added; MPEP 706.2)

Here, Applicants were unable to locate any teaching in this reference regarding a second region formed such that it encloses a first region. Instead, the Torii Publication appears to disclose a structure wherein emitter regions are formed intermittently, and the length of an emitter region increases as its distance to a gate bus line increases.

Such a configuration is fundamentally different from that of the claimed embodiments. In particular, as with a conventional device distinguished by the instant application, the device of the Torii Publication may eventually experience a thermal runaway effect due to the heat transmitted from the peripheral part of the center part, and the current capacity of the semiconductor device as a whole can decrease when a sufficient amount of current is not secured at the peripheral part.

Based at least upon the failure of the art relied upon by the Examiner to teach or even suggest all of the elements of the pending claims, it is respectfully asserted that no conclusion of anticipation can reasonably be drawn. Continued rejection of the pending claims is therefore improper , and the claim rejections should be withdrawn.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
KJT:k3a

61506370 v1